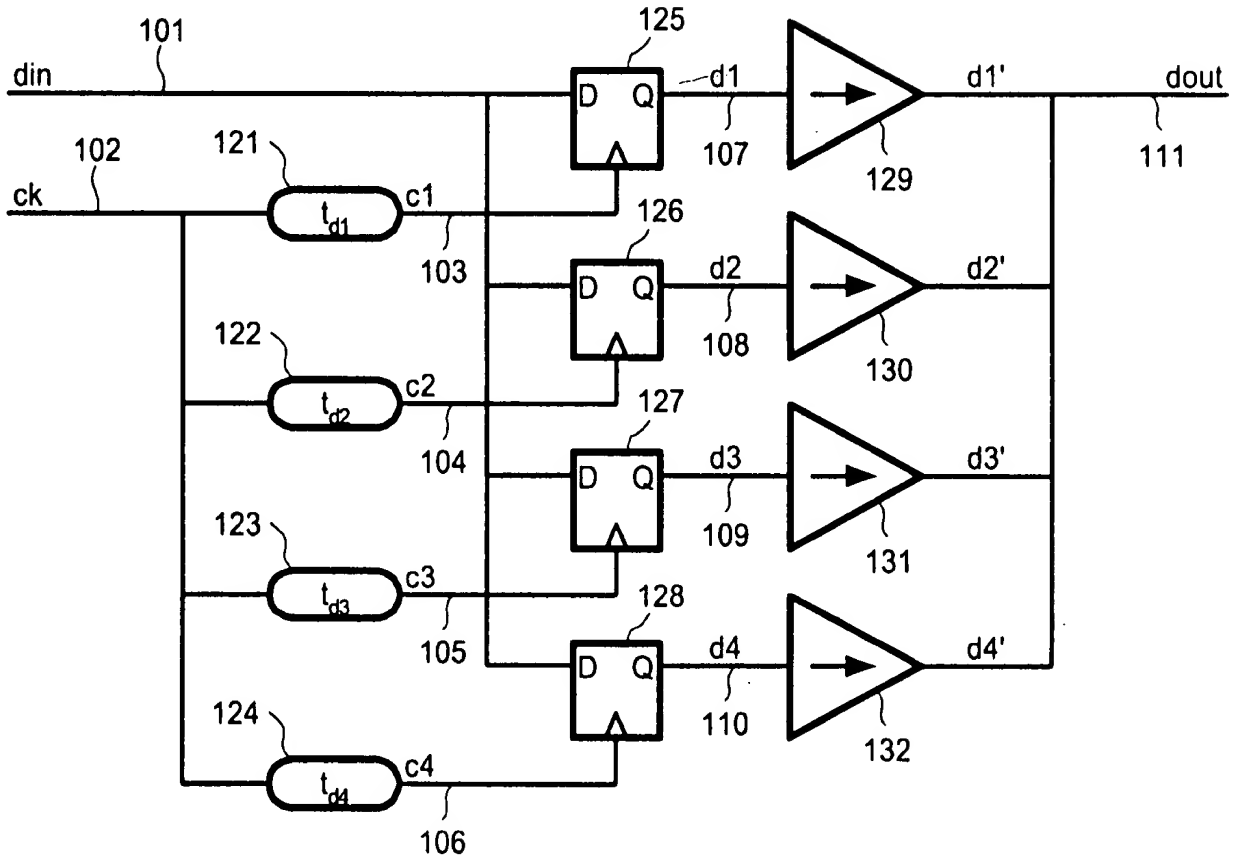
101
din
102
ck
121
t_{d1}
c1
103
122
t_{d2}
c2
104
123
t_{d3}
c3
105
124
t_{d4}
c4
106
125
D Q
d1
107
126
D Q
d2
108
127
D Q
d3
109
128
D Q
d4
110
129
130
131
132
d1'
d2'
d3'
d4'
dout
111

Figure 1

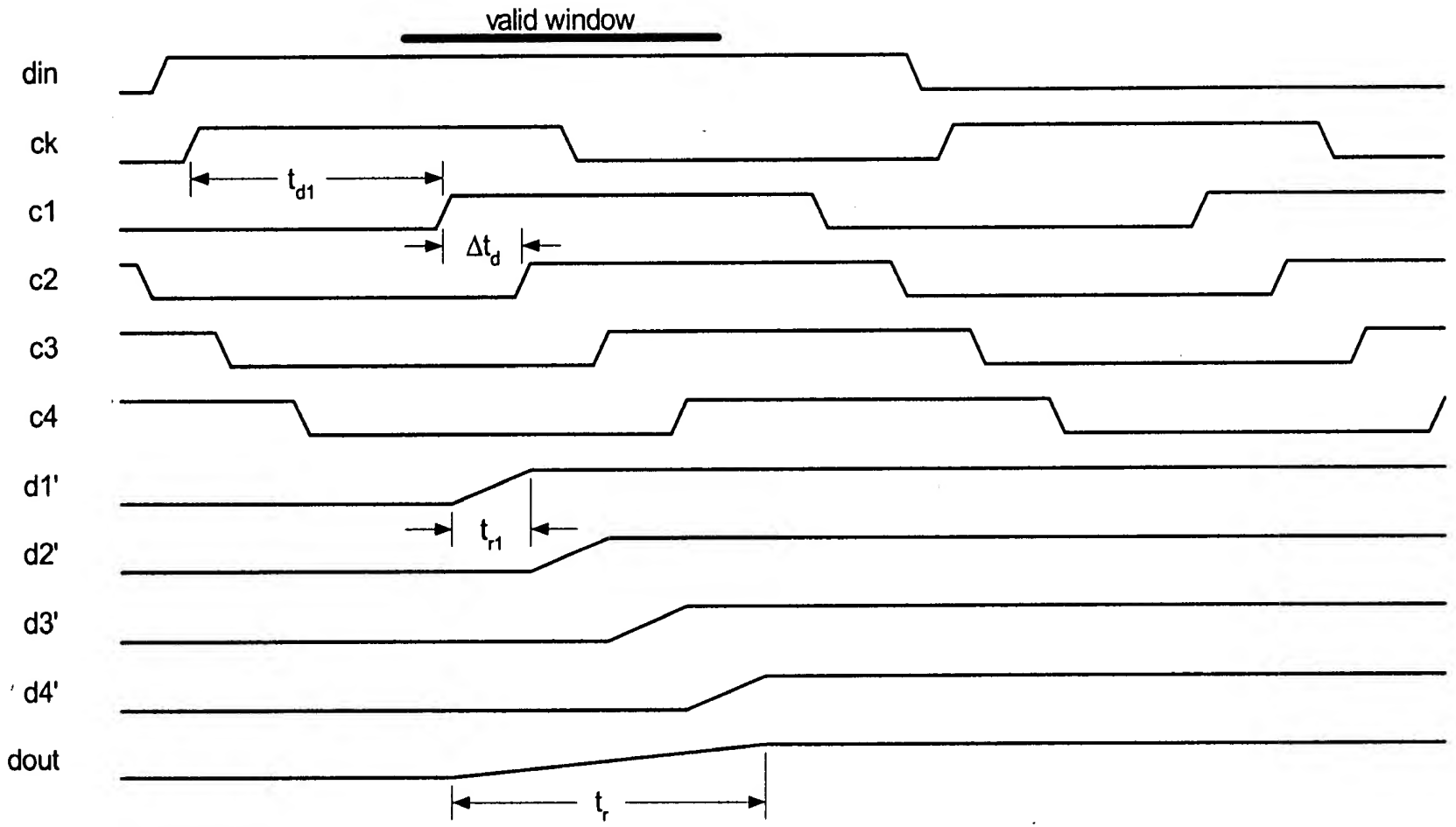
valid window
din
ck
c1
c2
c3
c4
d1'
d2'
d3'
d4'
dout
t_{d1}
Δt_d
t_{r1}
t_r

Figure 2

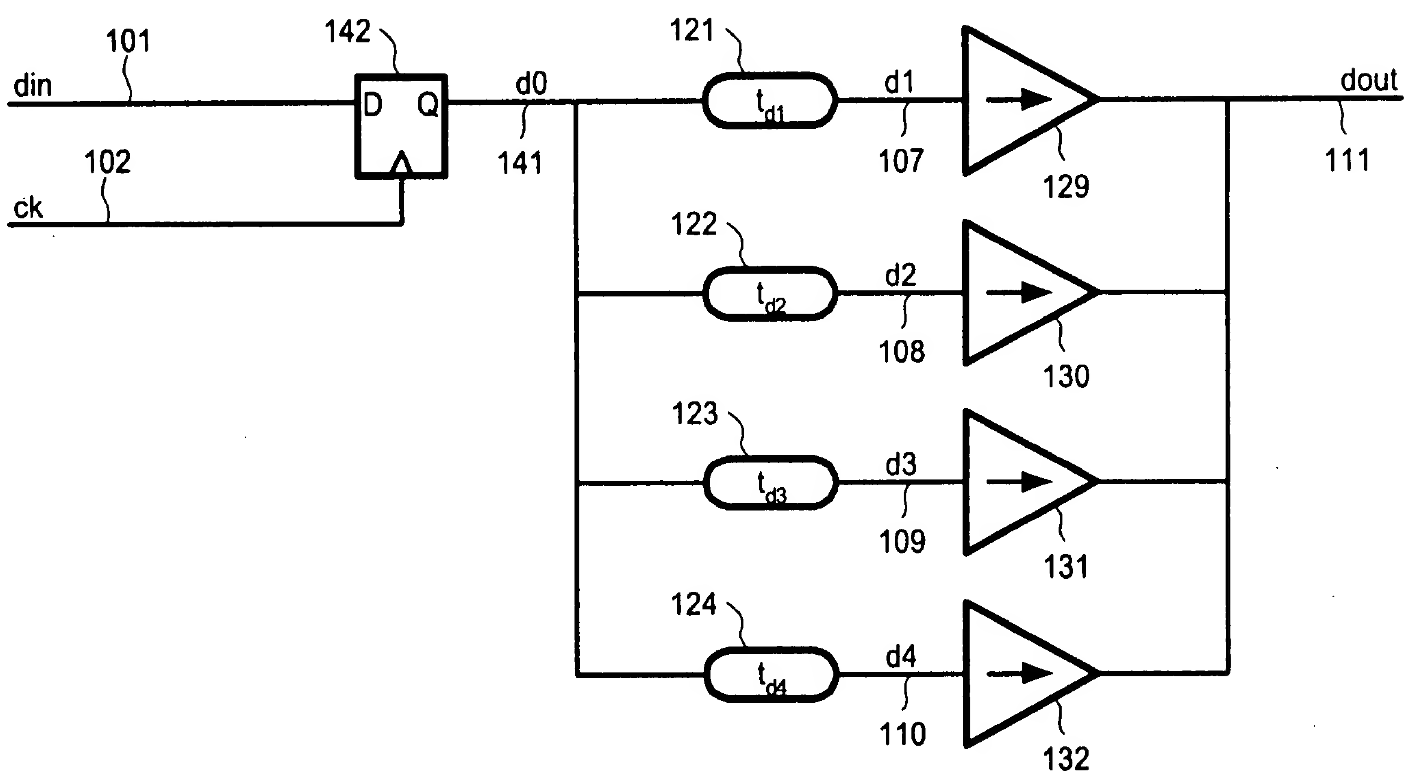
101
din
102
ck
142
D
Q
d0
141
121
t_{d1}
d1
107
129
122
t_{d2}
d2
108
130
123
t_{d3}
d3
109
131
124
t_{d4}
d4
110
132
dout
111

Figure 3

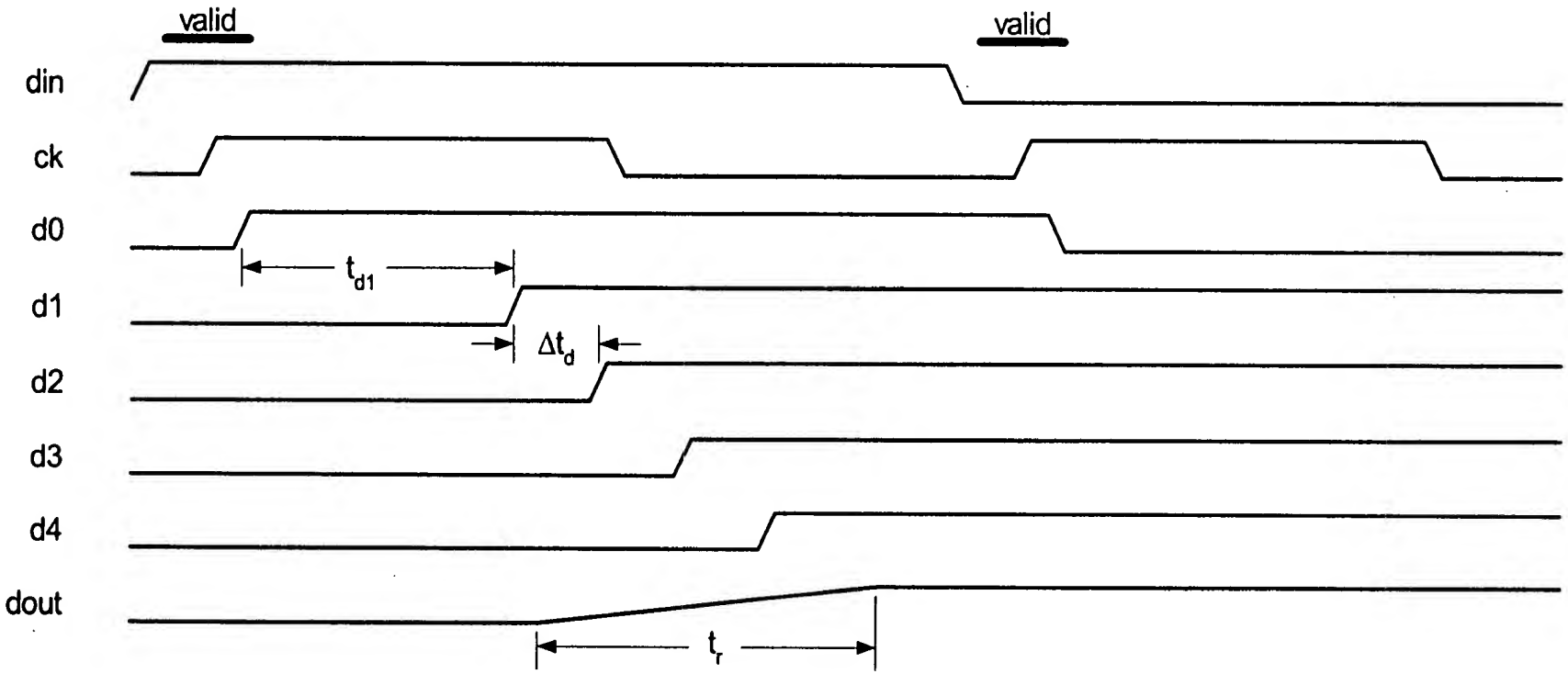

Figure 4

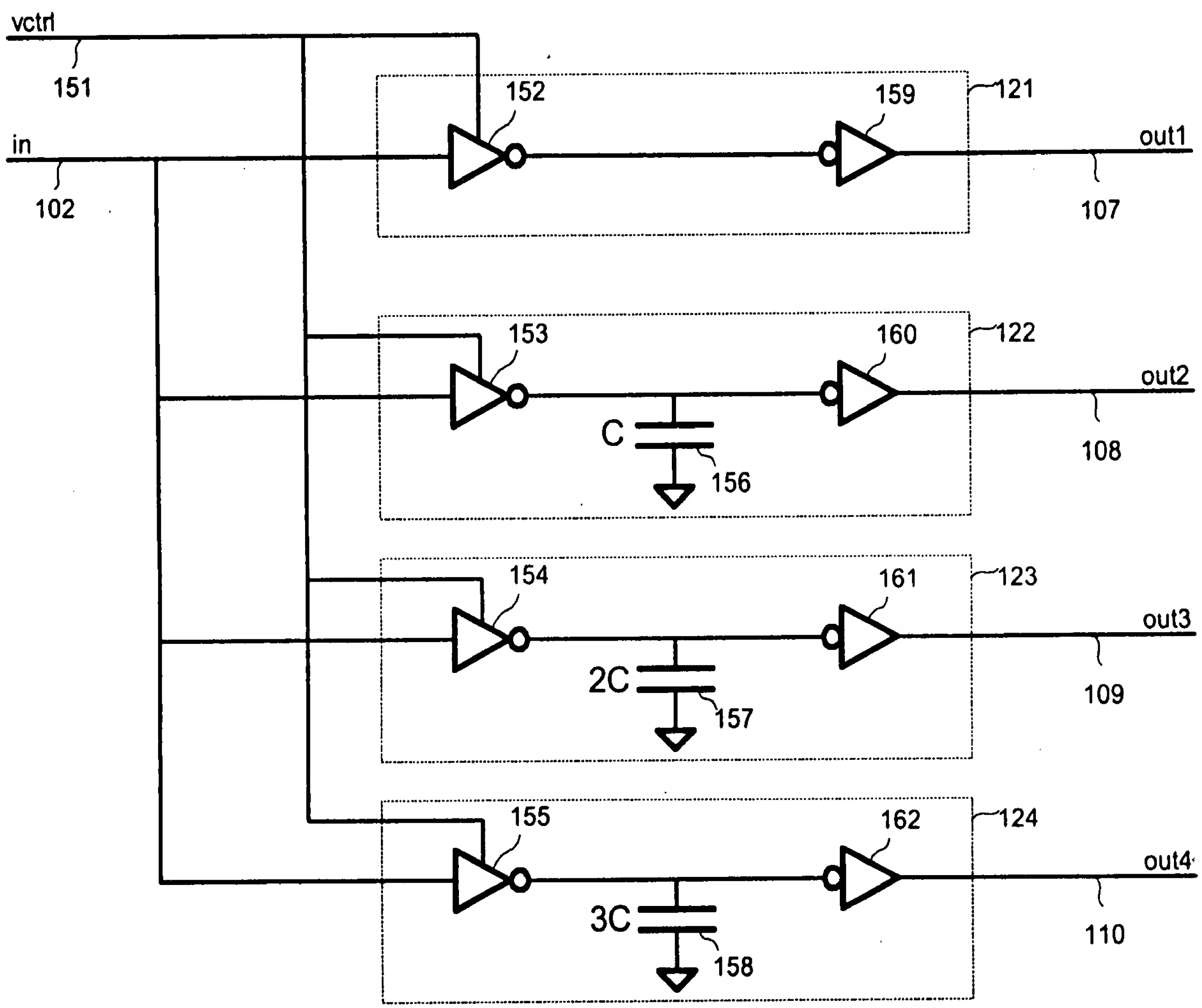
vctrl
151
in
102
152
159
121
out1
107
153
160
122
out2
C
156
108
154
161
123
out3
2C
157
109
155
162
124
out4
3C
158
110

Figure 5

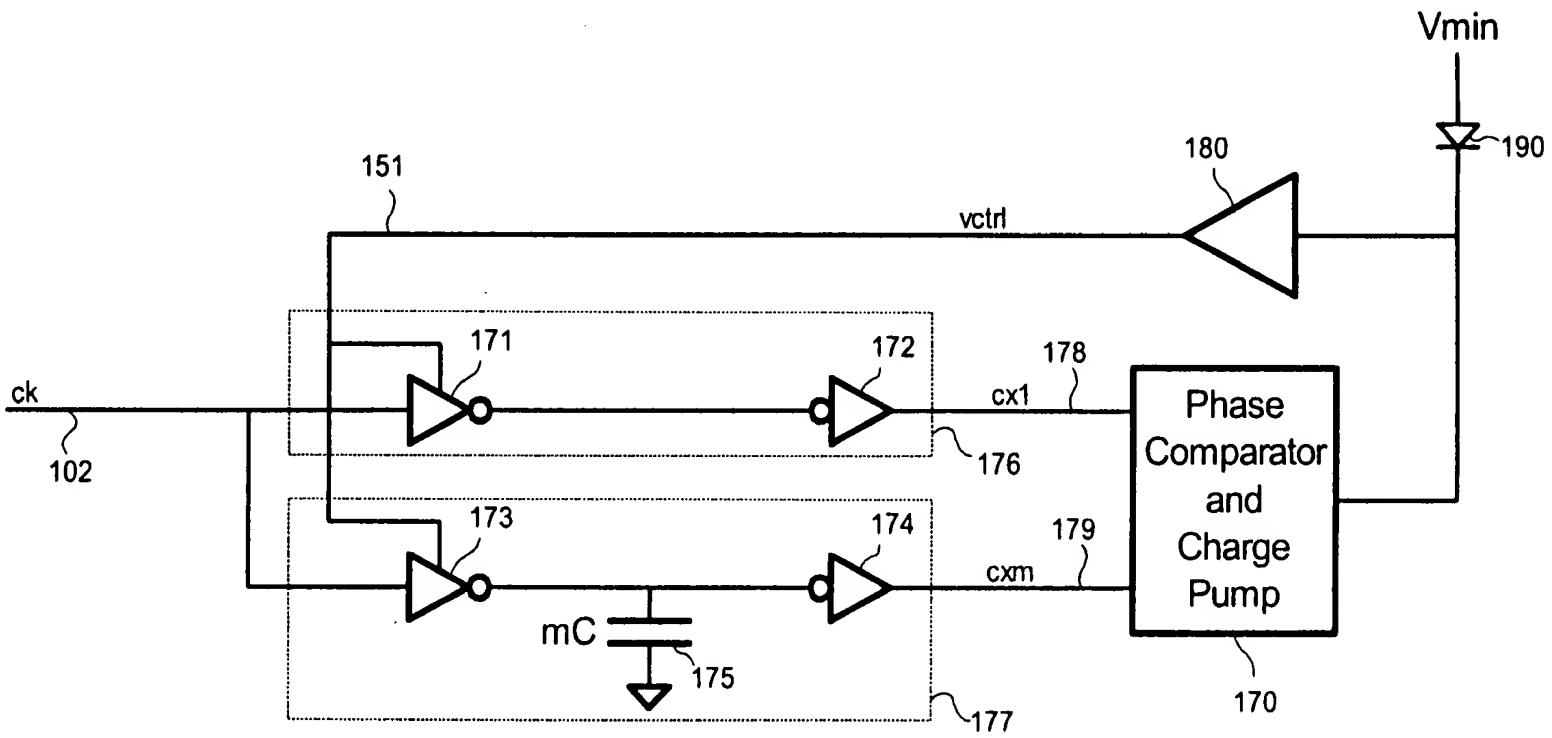
Vmin
190
180
151
vctrl
171
172
178
ck
cx1
102
176
Phase
Comparator
and
Charge
Pump
173
174
179
cxm
mC
175
177
170

Figure 6

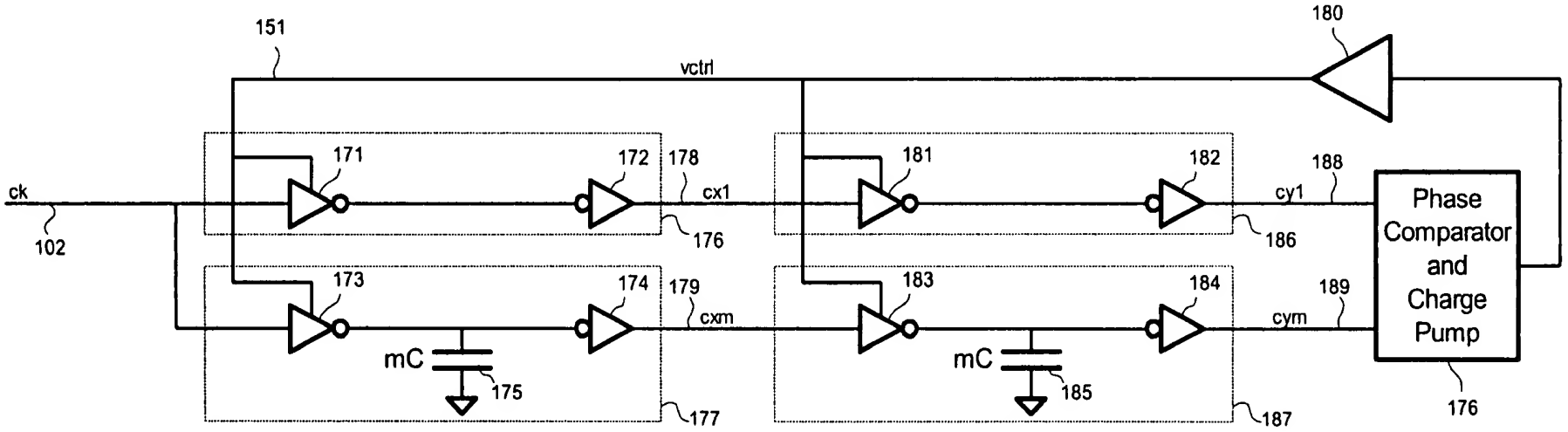
151
vctrl
180
171
172
178
cx1
181
182
188
cy1
ck
102
176
186
Phase
Comparator
and
Charge
Pump
173
174
179
cxm
183
184
189
cym
mC
175
177
mC
185
187
176

Figure 7

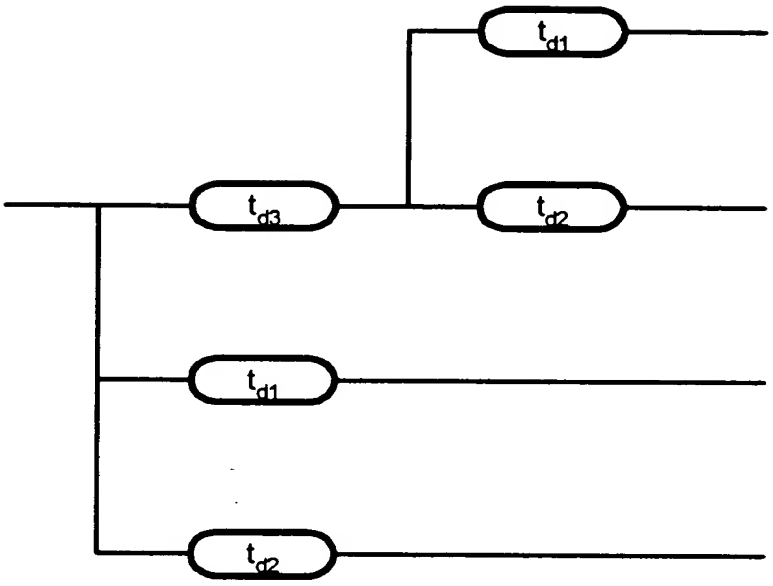

Figure 8